REMARKS

Original claims 1-24 are pending and are unamended.

Rejection - 35 U.S.C. § 112

The Examiner rejected claims 1, 2, 4-7, 9-10, 12-13, 15-18, and 20-24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner states that the limits for the parameters M, N, N_1, N_2 and B are not defined and specified clearly. Applicants respectfully traverse the rejection.

The parameters M and N are clearly defined at page 6, line 9 of the specification. The parameters N_1 and N_2 are clearly defined at page 10, lines 12-17 of the specification. The parameter B is clearly defined at page 7, line 21 of the specification. In view of the foregoing, Applicants request reconsideration and withdrawal of the § 112 rejection of claims

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 1, 2, 5, 9, 12, 13, 16, 20, 21 and 24 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,801,641 (Yang et al.) in view of U.S. Patent No. 4,955,017 (Eng et al.). Applicants respectfully traverse the rejection.

Yang et al. is directed to a controller for a broadcast switching network (Abstract). The switching network comprises an input stage of r_1 switches, each switch having n_1 input ports, an output stage of r_2 switches, each switch having n_2 output ports and a middle stage having m switches (Abstract).

Claims 1, 2, 5, 9, 12, 13, 16, 20, 21 and 24

Claim 1 reads as follows:

> *An M×N packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports, the switch comprising*
>
> *an input module, having M inputs and B outputs, B > M, for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times,*

a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, and

an output module, having B inputs and N outputs coupled to the packet buffer, for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets.

The Examiner states that Yang et al. discloses an MxN packet switch for switching M packets arriving in each of a sequence of frame times to N output ports and a packet buffer including B registers coupled to the input module for storing M switched packets into M available registers during each of the frame times. Applicants submit that the Examiner has mischaracterized Yang et al.

Yang et al. does not refer at any place to either "packets" or "frames". At col. 6, lines 34-38, Yang et al. refers to the need to transfer text/voice/video/graphics information and does not refer to this information being in the form of packets or being formatted into frames at col. 6 or at any place in the patent. Also, the references made by the Examiner (i.e. col. 3, lines 52-57 and col. 6 lines 54-61) refer only to the structure of the network and the controller of the network and do not teach or suggest that the network disclosed by Yang et al. switches packets arriving in a sequence of frame times and which stores M of the switched packets into M available registers during each of the frame times, as recited in claim 1.

The Examiner further refers to col. 11. lines 32-37 for the premise that Yang et al. discloses a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets. However, as clearly described in the Abstract and at col. 3, lines 51-57, the middle stage of the network disclosed by Yang et al. comprises switches and not registers for storing packets. Further, the text at col. 11, lines 32-37 clearly refers to middle switch state registers 70 which store information about which output links of the middle stage switches are idle (see col. 5, lines 53-58) and not to registers which store packets, as recited in claim 1.

The Examiner further states that Yang et al. does not expressly disclose transferring packets from occupied registers to output ports based on a destination address contained within

each stored packet but that Eng. et al. discloses at col. 2, lines 60-65 and col. 6, line 66 to col. 7, line 3 that transferring up to N packets from occupied registers in each of the frame times to the output ports based upon the network addresses with each of the stored packets.

Eng et al. discloses an NxN packet switch comprising a three-stage interconnection network, where each stage is composed of a plurality of switching modules. In operation, packets arrive simultaneously in a given time slot at the inputs to the input modules. The time slot is divided into M mini-slots, where M is the number of input modules. For each mini-slot, a separate particular output packet switch is assigned, or mapped, to each input module. Each input module then examines the destination address in each packet received during the time slot and determines which packets are destined for the particular output packet switch assigned to the input module during each particular mini-slot. (column 4, line 9 to column 7, line 58). A path is then reserved from the first stage to the second stage and from the second stage to the third stage for each packet determined to be destined for a particular output (third stage) switch. The second stage is then responsible for providing a connection between the two paths (col. 4, lines 51-55).

Claim 1 recites an input module for switching M input packets, a packet buffer including B registers coupled to the input module for storing the M switched packets and an output module for transferring up to N packets from occupied registers to the output ports. As discussed above, Yang et al. does not teach or suggest a packet buffer coupled to the input module for storing M switched packets. Eng et al. does not make up for this deficiency.

Eng et al. discloses a second stage (intermediate stage) which is merely a switch which receives the switched packets from the first stage and routes each of the packets from the output of the first stage to a selected input of the third stage based on a path determined by the routing algorithm. In contrast, the second (intermediate stage) of the present invention, as recited in claim 1, is a buffer stage for storing packets and does not perform the function of routing.

Applicants further submit that Yang et al. and Eng et al. are not properly combinable under 35 U.S.C. § 103. Yang et al. is directed to a circuit switching network for broadcasting continuous text/voice/video/graphic signals and not packet signals. In contrast Eng et al. is a packet switching system. Accordingly, if Yang et al. were modified to incorporate the function of transferring packets described by Eng et al. the modification would impermissibly change the

entire operation of the circuit switch described by Yang et al. and would likely make the Yang et al's. inoperable without wholesale modification of Yang et al's. switch.

The combination of Yang et al. and Eng et al. does not teach or suggest a packet switch having a packet buffer which accepts switched packets during each frame time from an input module and transfers the buffered switched packets to an output module in each of the frame times. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of claim 1.

Further, it is respectfully submitted that since claim 1 has been shown to be allowable, claims 2, 5 and 9 dependent on claim 1 are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 2, 5 and 9.

Independent claim 12 recites, *inter alia* ..."a packet switch comprising ...storage means, including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stores packets and output means coupled to the packet buffer for transferring up to N packets from occupied registers during each of the frame times"... Independent claims 21 and 24 each recite, *inter alia* ..."a method for switching ...comprising ....storing the M switched packets into M of B registers in each of the frame times to produce M stored packets, and transferring up to N packets from up to N of B registers in each of the frame times"...

As discussed above, the combination of Yang et al. and Eng et al. does <u>not</u> teach or suggest a packet switch having a packet buffer which stores switched packets during each frame time from an input module and which transfers the stored packets to an output module in each of the frame times as recited in each of claims 12, 21 and 24. Accordingly, for all the same reasons as recited for claim 1, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of independent claims 12, 21 and 24.

Further, it is respectfully submitted that since independent claim 12 has been shown to be allowable, claims 13, 16 and 20 dependent on claim 12, are allowable, at least by their dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 13, 16 and 20.

Rejection - 35 U.S.C. § 103

The Examiner rejected claims 3, 4, 6-8, 10-11, 14, 15, 17-19 and 22-23 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,801641 (Yang et al.) in view of U.S. Patent No. 4,955,017 (Eng et al.) and further in view of U.S. Patent No. 5,583,,861 (Holden). Applicants respectfully traverse the rejection.

Holden is directed to an ATM switching system comprising a switch fabric (Fig. 2) of a plurality of switch element circuits (Figs. 3 and 5) and routing table circuits (Abstract). Each switch element circuit includes a shared cell buffer pool (col. 2, lines 56-57). All cells passing though the switch element are written into the cell buffer pool during a first cell cycle and connected to the switch element output at a later cell cycle.

Claims 10 and 11

Independent claim 10 recites, *inter alia*, an MxN packet switch comprising a one-stop shared buffer memory. As defined on page 3 of the application, a one-stop buffer in the context of a packet switch, is a packet buffer such that whenever a packet occupies a register in the buffer, it remains in that register until its eventual exit from the packet switch.

Holden does not disclose, teach or suggest a one-stop buffer. The cell buffer pools disclosed by Holden are associated with each element of the switch fabric. As such, a packet is written and read from each cell buffer pool as the packet makes its way through the switch fabric. Thus, a packet does not remain in a single memory location over the entire time that the packet is transitioning through the switch and therefore the shared memory pool disclosed by Holden can not be characterized as a one-stop buffer.

Neither Yang et al. nor Eng et al. nor Holden disclose, teach or suggest a one-stop shared buffer memory as recited in independent claim 10. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of independent claim 10.

Further, it is respectfully submitted that since independent claim 10 has been shown to be allowable, claim 11 dependent on claim 10, is allowable, at least by its dependency. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claim 11.

Claims 3 and 14

Claims 3 and 14, dependent respectively on claims 1 and 12 each recite a one-stop packet buffer. Neither Yang et al. nor Eng et al. nor Holden disclose, teach or suggest a one-stop shared buffer memory as recited in dependent claim 3. Further, Holden does not teach or suggest a packet switch having a packet buffer which stores switched packets during each frame time from an input module and which transfers the stored packets to an output module in each of the frame times as recited in each of claims 1 and 12 and which is not taught by Yang et al. or Eng et al. Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of dependent claims 3 and 14.

Claim 23

Claim 23 recites, *inter alia,*

A method of switching M packets comprising:
transmitting the register address of the M available registers to header hoppers;
sending headers from the M input packets to the header hoppers,
transmitting the register address from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets,
updating the queues based on the header information provided by the header hoppers,
sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each of the frame times,
selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues,
transmitting the up to N selected stored packets to the outputs, updating the register selector to account for any remaining destination addresses for each stored packet, and
transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining packets.

The Examiner states that the combination of Yang et al. and Eng et al. do not disclose the limitations listed above but that Holden does disclose the limitations of claim 23 listed above at

Fig. 4, and col. 5, lines 38-46, col. 5, lines 46-51, col. 6, lines 32-43, and col. 7, lines 27-35 and col. 7 lines 46-56. Applicants respectfully disagree with the Examiner.

Holden's column 5, lines 38-46 describes the usage of a connection table controller for reading header information from the workstation interface and using that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Applicant's claimed subject matter does not include such connection table controllers. Holden's column 5, lines 46-51 describe an interrupt processor and processor interface, neither of which are claimed. Holden's column 6, lines 32-43 describes a cross point block, a bus controller, a link list RAM, a service order table, a memory for multicast group bits and a back pressure control circuit. Again not one of these elements is a limitation of claim 23. Col. 7 describes the use of a multipriority buffer pool controller (MPBPC) for controlling each switch element. Claim 23 does not include a limitation directed to a buffer pool controller.

One of many distinguishing features recited in claim 23 is the use of a "header hopper" for storing the addresses of available buffers and the headers of the input packets. One preferred embodiment of a header hopper is described on page 8, line 19 through page 9, line 10 and shown in Figs. 1 and 3. None of the discussion in Holden is related to the claimed "header hopper". Further, neither Yang et al., Eng et al. nor Holden has a component equivalent in function to Applicants' "header hopper."

Applicants submit that the combination of Yang et al., Eng et al. and Holden does not teach, suggest or disclose all of the limitations of claims 23. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §103 rejection of independent claim 23.

Claims 4, 6-8, 15, 17-19, and 22

Claims 4 and 6-8 depend from allowable claim 1. Claims 15, 17-19 depend from allowable claim 12. Claim 22 depends from allowable claim 21. It is respectfully submitted that since independent claim1, 12 and 21 have been shown to be allowable, claims 4, 6-8, 15, 17-19, and 22, dependent on claims 1, 12 and 21 are allowable, at least by their dependency.

Accordingly, for all the above reasons, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claim 4, 6-8, 15, 17-19, and 22.

Conclusion

Insofar as the Examiner's rejection has been fully addressed, the instant application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,
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(Date)

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